Transconductance/Drain Current Based Sensitivity Analysis for Analog CMOS Integrated Circuits

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***Abstract*— Recent studies have shown that transistor variability and ageing phenomena are responsible for variation of transconductance (g_m) and drain current (I_D) in MOSFETs. It is therefore important to perform sensitivity analysis at the earliest design stage in order to minimize effects of ageing. It is however not trivial to perform sensitivity analysis analytically because the I-V characteristics of modern transistors can not modeled without using complicated expressions. In this paper, We propose a technique that utilizes the transconductance-to-drain current ratio (g_m/I_D) of a transistor to captures the sensitivity of a circuit. This technique is applicable to transistors biased in all regions of operations. To explore the effectiveness of the proposed technique in practical circuit design, the sensitivity of a common source amplifier is analyzed. The proposed technique has an accuracy of ± 15 % between $4 < g_m/I_D < 28$.**

I. INTRODUCTION

In CMOS analog circuits, the minimum power consumption is achieved when transistors are operated in the weak inversion region [1]. In the absence of a compact equation that can be used to model the I-V characteristics of of MOSFETS in weak inversion, circuit designers often resort to circuit simulator in their design work. Over-reliance on circuit simulator can be problematic, potentially luring some engineers to develop the habit of diving into simulation without understanding basic circuit performance trade-offs. Jespers proposed a powerful transconductance-to-drain current (g_m/I_D) design technique to help designers to size up transistors quickly with good accuracy in [1].

The so called "g_m/I_D design approach" was useful for determining circuit parameters such as small signal gain and bandwidth. Building on Jespers' work, we have reported a g_m/I_D based noise analysis that utilized bias dependent thermal noise coefficient and device noise corner frequency to characterize device noise [2] and a technique to characterize transistor nonlinearity [3].

Recent studies have shown that variability and ageing phenomena are responsible for variation of g_m and I_D [6] and ultimately circuit reliability [5]. We are not aware of any published work linking a g_m/I_D analysis to g_m/I_D variation.

In this paper, we describe a g_m/I_D based approach to analyze circuit sensitivity. The goal of this study is to formulate a method that incorporates sensitivity analysis at the earliest design stage in order to minimize effects of variability and ageing. The emphasis is on formulating a g_m/I_D method that provides valuable insight and accuracy.

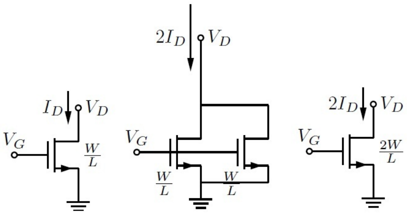

Fig. 1. Transistors biased at the same g_m/I_D ratio.

The organization of this paper is as follows. Section II provides an overview of the g_m/I_D analysis. Section III describes the sensitivity of a transistor in the context of g_m/I_D analysis. Section IV applies the g_m/I_D sensitivity analysis to a common source amplifier and compares the results of a hand calculation with BSIM4.4 model simulation in Cadence Spectre.

II. THEORY

A. Fundamentals

The g_m/I_D technique is applicable whenever we deal with a parameter that is independent of a transistor's width (W). Figure 1 shows a transistor with a transconductance of g_m, a drain-to-source conductance of g_{ds}, and a bias current of I_D, a gate-to-source voltage of V_{GS} and a drain-to-source of V_{DS}. If we connect an identical device in parallel with the stand-alone device so that both devices are biased at the same V_{GS} and V_{DS}, then both devices have the same g_m, g_{ds} and the same I_D with an aspect ratio of $2W/L$. The effective transconductance over current ratio is g_m/I_D for both the merged device and the stand-alone device because g_m and I_D are doubled. The drain-to-source conductance is doubled for the merged device, resulting in an intrinsic gain (g_m/g_{ds}) that is identical for both the stand alone device and the merged device. As long as transistors are biased at the same g_m/I_D, they will have the same g_m/g_{ds}, provided that they have the same L and V_{DS}. This observation is true for any two parameters whose ratio depend solely on the g_m/I_D and not on the width of a transistor. The list of parameters that do not depend on the

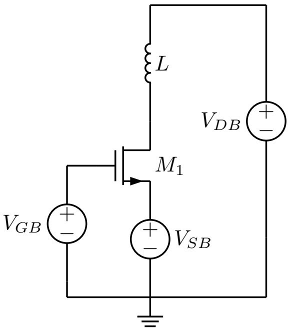

Fig. 2. Circuit used to determine the small signal parameter of the transistor at each g_m/I_D.

width of a transistor include current density, transit frequency, device noise corner frequency and thermal noise coefficient [2]. Once a transistor of a given width (W) is characterized over a range of g_m/I_D, the g_m/I_D based parameters can be generalized to a transistor of an arbitrary width. g_m/I_D methodology will hold as long as the parameter of interest scales with W.

B. Parameter Extraction Via Interpolation

We describe a procedure for obtaining g_m/I_D parameters from a design kit in this section. Transistors from IBM's CMRF8SF 0.13 μm CMOS process are used in this paper. Transistors are modeled using BSIM4.4. Cadence's Spectre simulator is used to determine the DC operating point of a transistor. Figure 2 shows the schematic used to generate the g_m/I_D database. Bias dependent small signal parameters of M_1 is obtained by changing the gate-to-bulk voltage (V_{GB}), the drain-to-bulk voltage (V_{DB}), the source-to-bulk voltage (V_{SB}) and length (L) of M_1. The bulk terminal is connected to ground. g_m/I_D is proportional to $1/(V_{GS} - V_{th})$ and can be set by using appropriate combinations of V_{GB} and V_{SB}. V_{SB} affects small signal parameters such as g_{mbs}, the body transconductance, therefore V_{SB} is changed to evaluate its impact on the small signal parameters when the source terminal is not tied to ground. V_{DB} causes channel length modulation and can be changed to evaluate its impact on small signal parameters. An inductor with an artificially large value (i.e. 1 GH) is inserted between the drain terminal of the transistor and V_{DB} power supply to provide DC bias to the drain terminal of M_1 and to avoid loading the output resistance of M_1. The length of an MOS transistor is changed in order to explore the length dependence of transistor parameters.

A typical analog circuit uses many devices, each biased under a different condition. It is not efficient to simulate small signal parameters for all possible combinations of g_m/I_D, V_{DS}, and L. The alternative is to create a database which stores values of a small signal parameter at specified values of g_m/I_D, V_{DS}, and L and interpolate that database as necessary. Figure 3 illustrates this process, where γ represents a parameter of interest for a given g_m/I_D. γ_G is the value of γ at $V_{DS} = 0.28$ V and $V_{SB} = 0.13$ V. γ_A, γ_B, γ_C, γ_D are values of γ in the database. To get γ_G, we interpolate γ_A and γ_B to obtain γ_F, γ_C and γ_D to obtain γ_E, and finally γ_E and γ_F to get γ_G. This process can be repeated to find γ of every transistor in the schematic.

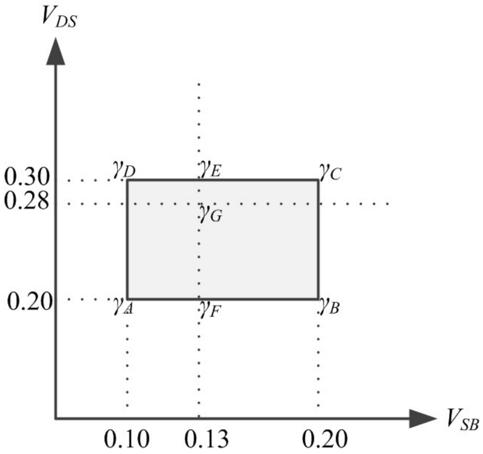

Fig. 3. Interpolation of γ at a specified g_m/I_D.

III. Device Sensitivity

In Section II, γ represents any g_m/I_D dependent parameters of a MOSFET, e.g. current density, transit frequency, the self-gain of an amplifier (g_m/g_{ds}). In this section, we choose g_m/g_{ds} to demonstrate the sensitivity of γ on its g_m/I_D. Section IV correlates the sensitivity of g_m/g_{ds} with the voltage gain of a common source amplifier.

A. Self Gain (g_m/g_{ds})

The output resistance ($1/g_{ds}$) of an MOS transistor is associated with the variation of drain to source voltage (V_{DS}). An incremental increase of V_{DS} leads to an incremental increase of the reverse bias voltage of the depletion region around the drain, and hence a slight increase in the the width of the depletion region. The effective length of the channel is reduced as the width of the depletion region is increased. The resulting incremental increase in I_D in response to an incremental increase in V_{DS} is modeled by an output resistance equal to

$$\frac{1}{g_{ds}} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{\lambda I_D}, \tag{1}$$

where λ is a channel length modulation parameter. It should be pointed out that λ depends on L as well as V_{DS}. The exact value of λ is usually not required in the g_m/I_D design flow since designers are usually more interested in the numerical value of g_m/g_{ds}.

Figure 4 shows the g_m/g_{ds} versus g_m/I_D for an NFET biased at $V_{DS} = 0.6$ V and $V_{SB} = 0.1$ V for $L = 1$ μm.

A transistor operating in the subthreshold region typically has a $g_m/I_D > 25$ and a transconductance equal to [4]

$$g_m = \frac{I_D}{V_T} \frac{C_{ox}}{C_{js} + C_{ox}}, \tag{2}$$

where C_{ox} is the oxide capacitance and the C_{js} is the depletion capacitance. Since both g_{ds} and g_m are both proportional to I_D

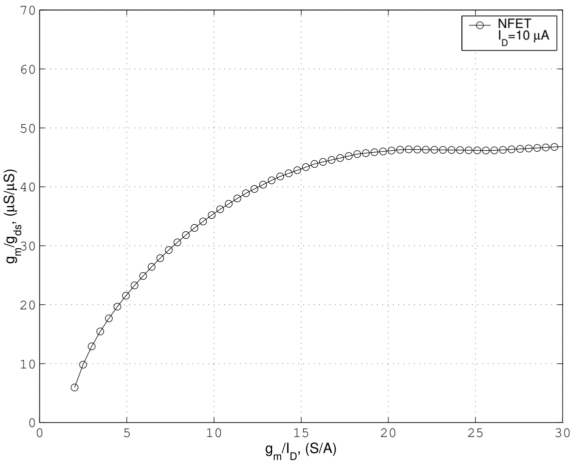

Fig. 4. Evaluation of g_m/g_{ds} as a function of g_m/I_D for $L = 1$ μm, $V_{DS} = 0.6$ and $V_{SB} = 0.0$.

for a device biased in the subthreshold region, the g_m/g_{ds} ratio is a constant independent of bias current as well as g_m/I_D. The flat region of the g_m/g_{ds} curve ($g_m/I_D > 25$) in Fig. 4 corresponds to the transistor operating in the subthreshold region.

A transistor operating in the strong inversion region typically has a g_m/I_D less than 10 and a transconductance equal to

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})(1 + \lambda V_{DS}). \tag{3}$$

Since $V_{GS} - V_{th}$ of a transistor is inversely proportional to g_m/I_D, the g_m/g_{ds} for a transistor operating at constant I_D is inversely proportional to g_m/I_D for a transistor in strong inversion. This explains the linear slope of g_m/g_{ds} at low g_m/I_D in Fig. 4. Between $g_m/I_D = 10$ and $g_m/I_D = 20$, the transistor is in weak-inversion, the slope is neither linear nor zero. The typically square law expression does not model the transistor behavior in this region with sufficient accuracy.

B. Sensitivity of g_m/g_{ds}

The sensitivity of any circuit variable y to a parameter x is defined as [4]

$$S_x^y = \frac{x}{y}\frac{\delta y}{\delta x}. \tag{4}$$

If we substitute y by g_m/g_{ds} and x by g_m/I_D, we have the sensitivity of g_m/g_{ds} with respect to g_m/I_D,

$$S_{g_m/I_D}^{g_m/g_{ds}} = \frac{g_m/I_D}{g_m/g_{ds}} \frac{\delta(g_m/g_{ds})}{\delta(g_m/I_D)}. \tag{5}$$

$S_{g_m/I_D}^{g_m/g_{ds}}$ is proportional to the first derivative of g_m/g_{ds} with respect to g_m/I_D. The sensitivity of g_m/g_{ds} as a function of g_m/I_D is shown in Fig. 5. The transistor is sensitive to g_m/I_D at lower g_m/I_D values because g_m/g_{ds} changes rapidly with g_m/I_D. As g_m/g_{ds} becomes independent to g_m/I_D at larger g_m/I_D values, $S_{g_m/I_D}^{g_m/g_{ds}}$ is reduced close to 0.

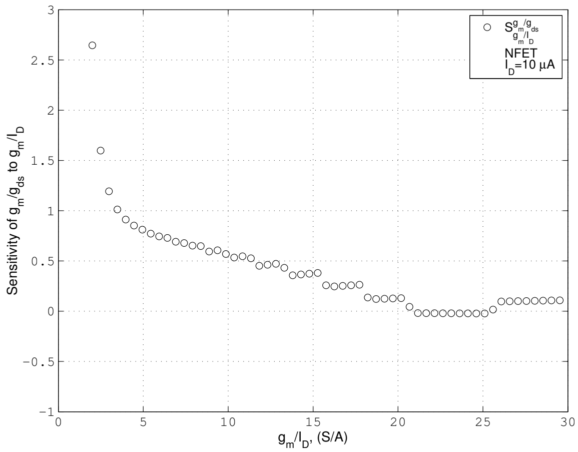

Fig. 5. Sensitivity of g_m/g_{ds} to g_m/I_D for $L = 1$ μm, $V_{DS} = 0.6$ and $V_{SB} = 0.0$.

IV. DESIGN EXAMPLE

A. Analysis of a Common Source Amplifier

A common source amplifier is analyzed in this section (Fig. 6) to illustrate first the sensitivity of the amplifier gain and second the process of minimizing gain sensitivity by choosing the g_m/I_D carefully. The voltage gain ($|A_V|$) of a common source amplifier is

$$\frac{1}{|A_V|} = \frac{1}{g_m R_D} + \frac{1}{\frac{g_m}{g_{ds}}} \tag{6}$$

Equation 6 has the form of the formula for calculating the effective resistance of two resistors in parallel, therefore the A_V is determined primarily by the smaller of g_m/g_{ds} and $g_m R_D$. Equation 6 can be re-written to shown the dependence of $|A_V|$ on g_m/I_D, as

$$\frac{1}{|A_V|} = \frac{1}{\frac{g_m}{I_D} I_D R_D} + \frac{1}{\frac{g_m}{g_{ds}}} \tag{7}$$

Equation 7 can be more compactly written with the following substitutions: $a = \frac{g_m}{I_D}$, $c = I_D R_D$, and $b = \frac{g_m}{g_{ds}}$. b is a function of g_m/I_D, therefore a function of a.

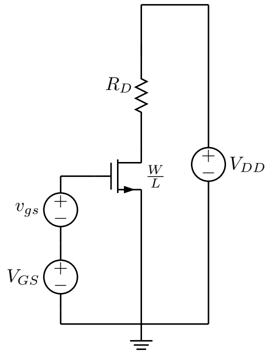

Fig. 6. An illustration of common source amplifier.

$$\frac{1}{|A_V|} = \frac{1}{ac} + \frac{1}{b} \tag{8}$$

Equation 8 can be further simplified to the following form:

$$|A_V| = \frac{acb}{b + ac} \tag{9}$$

The sensitivity of $|A_V|$ as a function of a (or alternatively g_m/I_D) is by definition

$$S_a^{|A_V|} = \frac{d|A_V|}{da}\frac{a}{|A_V|}. \tag{10}$$

Taking the first derivative of $|A_V|$ with respect to a, we have

$$\frac{d|A_V|}{da} = \frac{b^2c + a^2c^2\frac{db}{da}}{(b + ac)^2} \tag{11}$$

Substituting Eqn. 11 and Eqn. 9 in Eqn. 10, we have a compact expression for the sensitivity of the common source amplifier as a function of g_m/I_D ($a = g_m/I_D$), as

$$S_a^{|A_V|} = |A_V|(\frac{1}{ac} + \frac{1}{b}S_a^b). \tag{12}$$

B. Design Implications

In order to design a common source amplifier with low sensitivity to g_m/I_D, a is chosen carefully. Figure 5 shows that the g_m/g_{ds} sensitivity approaches the minimum when $20 < g_m/I_D < 25$. Figure 4 shows that g_m/g_{ds} is maximized when $20 < g_m/I_D < 25$. g_m/I_D is chosen to be 20.05 in order to minimize $S_{g_m/I_D}^{g_m/g_{ds}}$ and minimize effects of ageing. R_D is chosen to satisfy the gain require. Since the g_m/I_D of the transistor is fixed, $S_a^{|A_V|}$ can only be reduced at the expense of a larger I_D.

C. Results

We evaluate the accuracy of the proposed technique with a common-source amplifier. The bias current of the amplifier is chosen to be 10 μA. The length of the transistor is 1.0 μm. The g_m/I_D of the transistor is chosen to be 20.05 in order to reduce $S_a^{|A_V|}$ and maximize g_m/g_{ds}. The drain-to-source voltage of the transistor is fixed at 0.6 V. The current density (which depends primarily on g_m/I_D and V_{DS}) is obtained from the g_m/I_D database using the interpolation technique presented in Section II-B. The sensitivity of g_m/g_{ds} to g_m/I_D at g_m/I_D of 20 is 0.127 from Fig. 5. The sensitivity of the common source amplifier is calculated using Eqn. 12.

The gain of the common-source amplifier is simulated using BSIM4.4 model as follows: first, the W/L ratio is chosen to obtain a g_m/I_D of 20.05. The gain of the common source amplifier is 9.18, indicating that the gain (i.e. $|A_V| = 9.54$) determined using Eqn. 9 is off by 3.9 %. To mimic a small deviation in g_m/I_D from 20.05 to 20.2, the width is increased slightly and the V_{GS} is reduced slightly to keep I_D constant. The decrease in current density increases the g_m/I_D, leading to a gain of 9.24 according BSIM4.4 and a gain of 9.60 according Eqn. 10 (keeping the same estimation error). Using $|A_V|$ obtained from BSIM4.4 simulations, the expected $S_{g_m/I_D}^{|A_V|}$ is 0.86. Using the design technique proposed in this work, we found $S_{g_m/I_D}^{|A_V|} = 0.81$ presenting -5% of error.

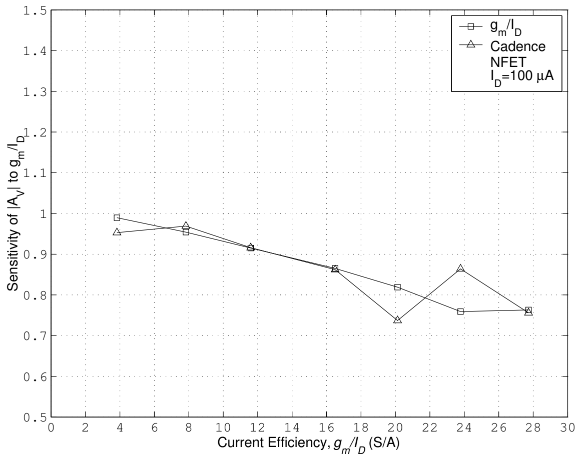

Fig. 7. Comparison of g_m/I_D analysis with BSIM4.4 simulations in Spectre for $V_{SB} = 0$V, $V_{DS} = 0.6$V and $L = 1\mu$m.

To generalize the results over a broad range g_m/I_D, the transistor's g_m/I_D over a broad range. The bias current is increased to 100 μA in order to keep the W above the W_{min} of the process at lower g_m/I_D values. The sensitivity of $|A_V|$ with respect to g_m/I_D is calculated and shown in Fig. 7. The percentage error is within ± 15 percent between g_m/I_D from 4 to 28.

V. CONCLUSION

We proposed a technique to analyze circuit sensitivity in analog CMOS integrated circuits. The proposed technique utilizes the transconductance-to-drain current ratio (g_m/I_D) of a transistor to capture a circuit's sensitivity due to a slight change in the bias condition. The technique described in this paper can be used to minimize transistor variability and ageing degradation. To explore the effectiveness of the proposed technique in practical circuit design, the sensitivity of a common source amplifier gain is analyzed. The proposed technique is shown to be accurate to within ± 15 % over a wide range of g_m/I_D.

REFERENCES

[1] F. Silveira, D. Flandre, and P. G. A. Jespers, "A g_m/I_D based methodology for the design of CMOS analog circuits and its application to the synthesis of a Silicon-on-Insulator micropower OTA," IEEE Journal of Solid-State Circuits, vol. 31, No.9, pp. 1314-1319, September 1996.

[2] Ou, J., "g_m/I_D based noise analysis for CMOS analog circuits," Circuits and Systems (MWSCAS), 2011 IEEE 54th International Midwest Symposium on, pp.1-4, 7-10 Aug. 2011.

[3] Ou, J., "Transconductance/Drain Current Based Distortion Analysis for CMOS analog circuits," 10th International NEWCAS Conference, June. 2012.

[4] Gray, P., Hurst, P., Lewis, S., and Meyer, R., Analysis and Design of Analog Integrated Circuits, 5th edition, Wiley, 2009.

[5] Maricau, E., Gielen, G., "Computer-Aided Analog Circuit Design for Reliability in Nanometer CMOS," IEEE Trans. Emerg Select Topics Circ. Syst., vol. 1, No.1, pp. 5058, March 2011.

[6] Ferreira, P. M., Petit, H., Naviner, J., "A New Synthesis Methodology for Reliable RF front-end Design",Circuits and Systems (ISCAS), 2011 IEEE International Symposium on, pp. 2926-2929, May 2011.