Implications of Small Geometry Effects on g_m/I_D Based Design Methodology for Analog Circuits

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***Abstract*—Small geometry effects have become increasingly important in analog circuits as transistors continue to shrink. As a result, transconductance-to-drain current (g_m/I_D) transistor parameters are no longer width-independent. In this brief, a procedure to develop "unit-sized" transistors with minimal sensitivity to small geometry effects is proposed. It is shown that by using the unit-sized transistors, the impact of small geometry effects on g_m/I_D dependent parameters such as current density and self gain can be reduced to 3.6% and 1.5%, respectively.**

***Index Terms*—g_m/I_D design approach and small geometry effects.**

I. Introduction

THE SO called "g_m/I_D design approach" was originally developed by Silveira *et al.* as a sizing tool with the premise that current density is width-independent and is dependent on the ratio of transconductance over DC drain current (g_m/I_D) [1]. The design methodology was validated in a long channel process and showed excellent correspondence with the predicted data [1]. As transistor dimensions continue to shrink, small geometry effects such as inverse narrow width effect (INWE) [2], [3], reverse short channel effect (RSCE) [4], and shallow trench isolation (STI) induced stress [5]–[8] have become increasingly important in analog design. There is, hence, a need for incorporating the impact of small geometry effects in the g_m/I_D design flow.

Sameer *et al.* [9] introduced an automated post circuit design strategy that minimizes STI induced stress while Zhang *et al.* [10] developed a circuit synthesis technique which uses geometric programming to minimize the effects of STI induced stress, the well proximity effect and RSCE. Ou *et al.* [11] presented a sophisticated analog layout placement technique that accounts for layout dependent effects. However, there remains a need for a less computationally intensive approach for incorporating small geometry effects in the analog circuit design flow.

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"Unit-sized" transistors are elementary transistors that can be connected in parallel to form larger transistors with well-understood characteristics in analog circuit design [12]. In this brief, we describe a method to develop "unit-sized" transistors with minimal sensitivity to INWE, RSCE, and STI induced stress. It is shown that by using the "unit-sized" transistors, g_m/I_D parameters such as current density and self-gain remain width-independent. g_m/I_D design approach remains valid. Small geometry effects can be minimized without using sophisticated sizing algorithms discussed in [9] and [10]. The "unit-sized" transistors do not account for the well proximity effect and the oxide-to-oxide spacing effect; these effects can be minimized during layout using best layout practice techniques described in [5] and [13].

The rest of this brief is organized as follows: In Section II, we review small geometry effects and discuss their implications on g_m/I_D design parameters. In Section III, we discuss the process of designing the "unit-sized" transistors with minimal sensitivity to small geometry effects. In Section IV, we use the "unit-sized" transistors to implement circuits known to be sensitive to small geometry effects and show that by using the "unit-sized" transistors, sensitivity to small geometry effects such as stress can be reduced. Finally, we present our conclusions in Section V.

II. Fundamentals

A. g_m/I_D Principle

The g_m/I_D design principle is applicable to parameters that are independent of a transistor's width. Once a transistor of a given width (W) is characterized over a range of g_m/I_D, g_m/I_D dependent parameters such as current density can be used to quickly size up transistors, assuming that the length remains constant [1].

B. Small Geometry Effect

As transistors continue to shrink, small geometry effects such as inverse narrow width effect (INWE), reverse short channel effect (RSCE), and shallow trench isolation (STI) induced stress have become increasingly important in analog design.

1) Inverse Narrow Width Effect: INWE is caused by parasitic fringing capacitances between the gate, the STI sidewall and the active area [2]. INWE is present in processes where "fully recessed" isolation or "shallow-trench isolation" is used [14]. The fringing field helps make the depletion region deeper and lowers V_{GS} required to deplete the channel before

an inversion layer can be formed. The threshold voltage is reduced as W is reduced [2], [14].

Akers shows that the threshold voltage shift for a transistor in a fully recessed isolated process is [15]

$$\Delta V_{th} = \frac{qN_aW_d}{C_{ox}} \frac{W}{W+F}, \tag{1}$$

where N_a is the channel doping concentration, W_d is the depth of the gate-induced depletion region, and C_{ox} is the thin gate oxide capacitance per unit area. F is a fringing factor defined as

$$F = \frac{4T_{ox}}{\pi} \ln\left(\frac{2T_d}{T_{ox}}\right), \tag{2}$$

where T_d is the thickness of the field oxide and T_{ox} is the thickness of the gate oxide. Equation 1 shows that ΔV_{th} is increased as W is increased and becomes $\frac{qN_aW_d}{C_{ox}}$ for $W >> F$. INWE is especially important in circuits designed to operate close to the threshold voltage. Since V_{th} is width dependent in devices affected by INWE, g_m/I_D parameters (e.g., current density) collected using the procedure described in Section II-A become width dependent and cannot be generalized to transistors of arbitrary widths.

2) STI Induced Stress: The STI induced stress is caused by the difference between the thermal expansion coefficients of the silicon and the STI oxide [6] and can be resolved into a longitudinal component along L (S_l) and a transversal component along W (S_t) [7]. It affects the carrier transport properties and produces a fractional change in mobility

$$\frac{\Delta\mu}{\mu} = \Pi_l S_l + \Pi_t S_t, \tag{3}$$

where Π_l and Π_t are piezoresistance coefficients in the longitudinal and the transversal directions [8]. In addition to introducing changes to mobility, the STI stress introduces changes to band structures and brings variations to band edge, bandgap and effective density of states [7], which can be captured as threshold voltage shift using $\Delta V_{th} = K_v \Delta\mu/\mu$ [8], where K_v is a process dependent coefficient.

Li *et al.* [7] have shown that both S_l and S_t are increased as the longitudinal dimension along L and the transversal dimension along W of the active area are reduced. Consequently, the STI induced effects are expected to become more pronounced as the process scales [7].

At the circuit level, the shifts in V_{th} and mobility translate to geometry dependent current density, making it difficult to size up transistors using width-independent g_m/I_D parameters.

3) Reverse Short Channel Effect: The reverse short channel effect is observed in processes where a "halo" implant is used to reduce the penetration of the source/drain depletion region into the channel. The implant creates nonuniform substrate doping along the channel, increases the average substrate doping, and increases the threshold voltage as L is reduced [4].

The reverse short channel effect is commonly observed in modern short-channel technologies [14] and can be modeled

$$\Delta V_{th} = \frac{2Q_oK_o}{C_{ox}L}\left(1 - \exp^{-\frac{L}{K_o}}\right), \tag{4}$$

where K_o and Q_o are process parameters which determine the extent that V_{th} is increased as L is reduced [16]. Section III-C3 shows that to account for the RSCE effect, length specific g_m/I_D parameters should be generated.

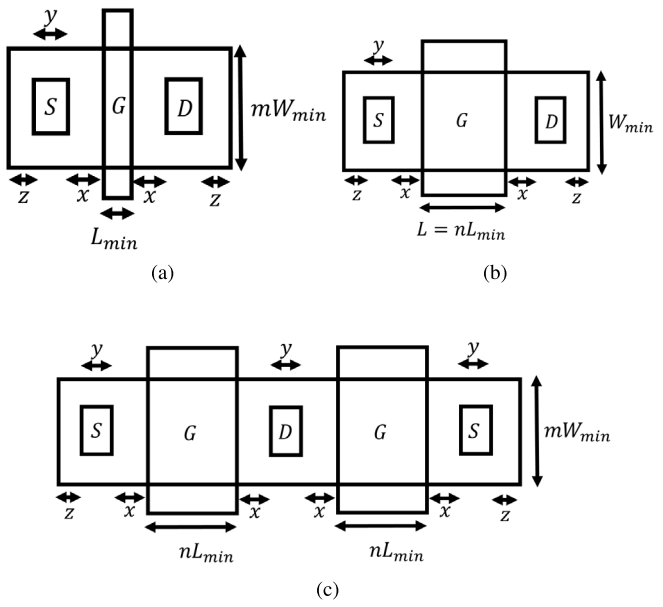


Fig. 1. Definitions of transistor parameters. W_{min} and L_{min} are minimum values of W and L. m and n are integer multipliers. V_G, V_S, and V_D are 0.45 V, 0.1 V, and 0.3 V respectively. x represents the distance from the gate to source/drain diffusion. y is the minimum horizontal dimension of source/drain diffusion. z is the distance from source/drain diffusion to the boundary of the active area. x, y and z are 260 nm, 240 nm and 100 nm respectively. (a) a transistor with $L = L_{min}$ and $NF = 1$. (b) a transistor with $W = W_{min}$ and $NF = 1$. (c) a multi-finger transistor with variable L and W.

III. Characterization of "Unit-Sized" Transistors

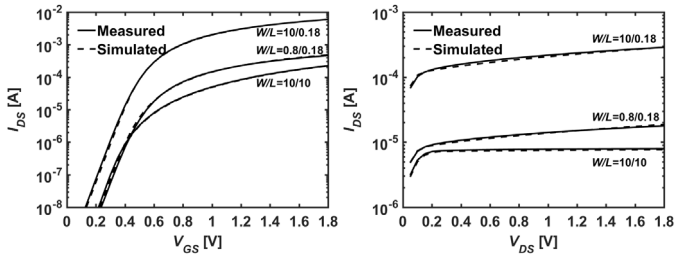
A. Definitions

Figure 1 illustrates geometries used to develop "unit-sized" transistors. A 180-nm CMOS process with a minimum length (L_{min}) of 180 nm and a minimum implementable width (W_{min}) of 400 nm is used. The normalized width (m) is defined as $m = W/W_{min}$. The normalized length (n) is defined as $n = L/L_{min}$. NF is the number of fingers.

B. Transistor Model

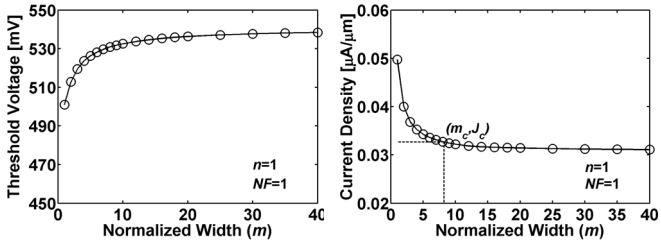
A design kit with transistors modeled using a scalable physics-based PSP 102.0 model is used [17], [18]. PSP 102.0 uses the same stress model as BSIM4.4.0 [17]. The STI stress effect is enabled by an optional global switch (`gstis`). By default, the STI effect is active (`gstis=1`) and can be turned off by setting `gstis` to 0 [18].

Measured drain currents are compared to simulated drain currents for three aspect ratios (10/10 μm/μm, 10/0.18 μm/μm and the 0.8/0.18 μm/μm) in order to evaluate model sensitivity of either W or L. Figure 2 shows general agreement between the measured and the simulated drain currents with maximum percentage errors of 5 percent and 6.5 percent respectively for the drain currents in Fig. 2(a) and the drain currents in Fig. 2(b).



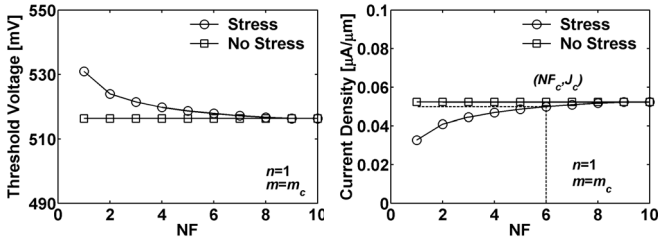
(a) (b)

Fig. 2. (a) I_{DS} as a function of V_{GS}. $V_{DS} = 1.8$ V. (b) I_{DS} as a function of V_{DS}. $V_{GS} = 0.6$ V, $V_{BS} = 0$ V, and $T = 25$ °C.



(a) (b)

Fig. 3. Width dependent (a) V_{th} and (b) J_D using the geometry and the bias condition described in Fig. 1(a).



(a) (b)

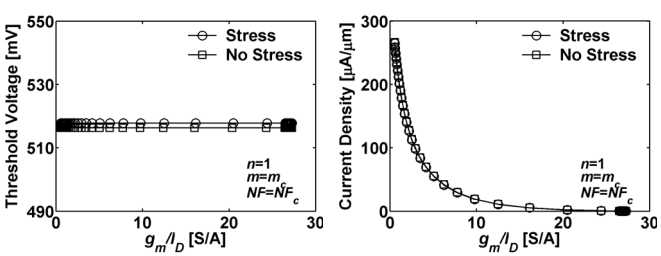
Fig. 4. Effect of stress on (a) V_{th} and (b) J_D of multi-finger transistors. The geometry and the bias condition are described in Fig. 1(c).

C. A Procedure for Developing Unit-Sized Transistors With Minimal Sensitivity to Small Geometry Effects

1) Determination of INWE: The extent of the inverse narrow width effect is evaluated by changing the normalized width (m) as illustrated in Fig. 1(a). Figure 3(a) shows that V_{th} is reduced as the normalized width (m) is reduced. Figure 3(b) shows that current density is increased as m is reduced since V_{GS} is constant. At $m = m_c$, Fig. 3(b) shows that the current density is 5 percent higher than the corresponding current density at $m = 40$.

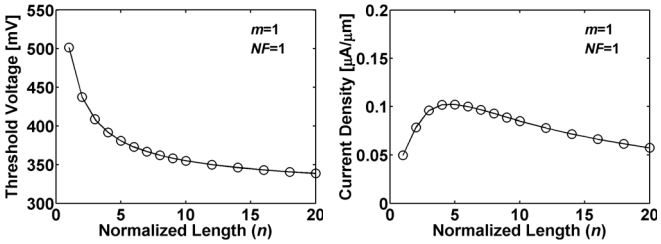
2) Effect of Stress: The stress parallel to the direction of the electron carriers is minimized by increasing NF (number of fingers) while keeping the width per finger constant. Figure 4 shows that by increasing NF, the effect of stress on threshold voltage and current density is minimized. At $NF = NF_c$, Fig. 4(a) shows that the current density is 5 percent below the corresponding current density at $NF = 10$.

Figure 5 shows the g_m/I_D dependence of a "unit-sized" transistor with a normalized length of 1, normalized width of m_c, and NF of NF_c. Figure 5(a) shows that regardless of



(a) (b)

Fig. 5. (a) V_{th} and (b) J_D as a function of the g_m/I_D of "unit-sized" transistors with $m = m_c$, $NF = NF_c$, and $n = 1$.



(a) (b)

Fig. 6. (a) V_{th} and (b) current density as a function of normalized width. The geometry and the bias condition are described in Fig. 1(b).

TABLE I
NORMALIZED WIDTH (m) AND NUMBER OF FINGERS (NF) ASSOCIATED WITH COMMONLY USED NORMALIZED LENGTH (n)

Application	High Speed	Moderate Gain/Speed	High Gain
n	1	2	5
m	8	5	6
NF	6	5	3

stress the threshold voltage is independent of its g_m/I_D, suggesting a one-to-one correspondence between V_{GS} and g_m/I_D. The shift in V_{th} due to stress is 2.1 mV for a g_m/I_D from 1 S/A to 27 S/A. Figure 5(b) shows that the shift in current density due to stress is minimal, suggesting that the sizing error associated with stress can be minimized when the "unit-sized" transistors are used.

3) Determination of RSCE: The extent of the reverse short channel effect can be evaluated by increasing the normalized length (n) while keeping the normalized width (m) constant as shown in Fig. 1(b). Figure 6(a) confirms that for $n \leq 5$, consistent with (4), the threshold voltage is increased as n is reduced. The current density is reduced (Fig. 6(b)) as the normalized length (n) is reduced [19]. For $n > 5$, the current density is reduced as L is increased.

The wide variation in current density and V_{th} across normalized lengths suggests that in order to account for RSCE at each n, the procedure described so far should be repeated to construct *length specific* "unit-sized" transistors that can be connected in parallel to build larger transistors. Table I shows the dimensions of three length specific "unit-sized" transistors that can be used for high speed ($n = 1$), moderate speed/gain ($n = 2$) and high gain ($n = 5$) applications.

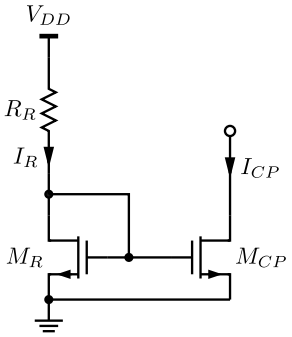


Fig. 7. A current mirror. The aspect ratio (W/L) for M_{COPY} is N times that of M_{REF}.

As discussed in Section II, RSCE, INWE and STI induced stress are commonly observed in modern processes. The procedure described in Section III-C is general and can be adopted in a different process to determine dimensions of "unit-sized" transistors.

IV. Design Examples

A. Current Mirror

Stress and small geometry effects discussed in Section III affect the output of current mirror circuits. Figure 7 shows a current mirror circuit with a normalized length of five. M_R has a normalized width of six and uses three fingers. M_{CP} is sized to be N times the aspect ratio of M_R. The stress option is enabled and disabled (simultaneously for both M_R and M_{CP}) in order to explore the impact on stress. The current ratio (N) is increased from 1 to 8 in order to assess whether the g_m/I_D parameters of M_{CP} are width independent.

Figure 8(a) shows a plot of I_{CP} as a function of stress and the current mirror ratio (N). The maximum discrepancy occurs at $N = 8$, where $I_{CP,stress} = 9.68\mu$A and $I_{CP,no\ stress} = 9.35\mu$A. The discrepancy (i.e., $|I_{CP,stress} - I_{CP,no\ stress}|$) is ≈ 3.4 percent of $I_{CP,stress}$. The current mirror is biased such that both transistors (M_R and M_{CP}) have the same V_{DS}. This result indicates that the "unit-sized" transistors developed in Section III can be used to minimize the effect of stress.

Figure 8(b) shows a plot of V_{th} as a function of stress and the current mirror ratio. Compared to Fig. 3(a), the threshold voltage of a 'unit-sized' transistor exhibits minimal sensitivity to stress and is width independent as N is increased.

Figure 8(c) shows a plot of the current density as a function of stress and the current mirror ratio. The largest discrepancy occurs at $N = 8$. With the current mirror ratio equal to 8, the current density under stress is 0.168 μA/μm and the current density obtained in the absence of stress is 0.162 μA/μm. The minimal deviation in current sensitivity indicates that the "unit-sized" transistor exhibits minimal sensitivity to stress. The current density under stress is flat for $N > 2$. This result indicates that the current density of the "unit-sized' transistor is width-independent and the "unit-sized" transistor can be used in a width-independent g_m/I_D design flow.

Both g_m (transconductance) and g_{ds} (drain-to-source conductance) are proportional to W and thus the self-gain, which is defined as g_m/g_{ds}, is a width independent g_m/I_D parameter.

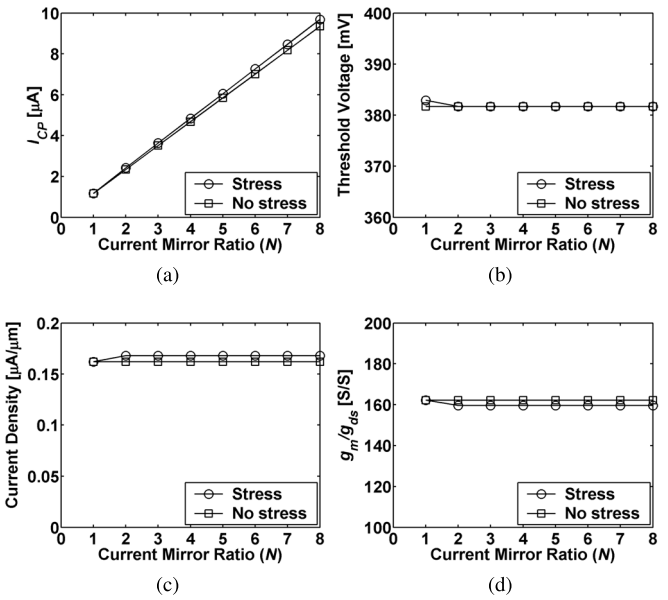


Fig. 8. Impact of stress and current ratio on I_{CP}. (a) I_{CP} as a function of stress and N. (b) Threshold voltage as a function of stress and N. (c) Current density as a function of stress and N. (d) Self-gain as a function of stress and N.

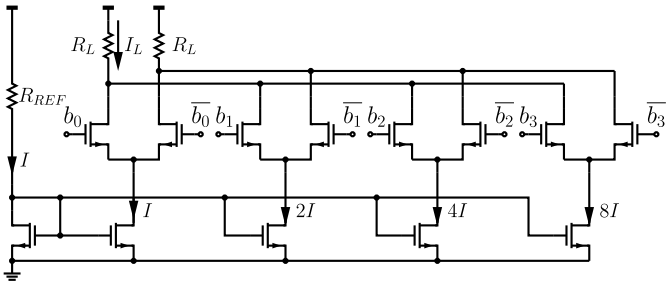


Fig. 9. 4-bit DAC developed using the current mirror in Fig. 7.

Figure 8(d) shows a plot of the self-gain of the "unit-sized" transistor. The largest discrepancy in self-gain occurs at $N = 8$. The self gain under stress is 159.6 and the self-gain obtained in the absence of stress is 162.1. The minimal discrepancy in self-gain indicates that the "unit-sized" transistor is not sensitive to stress. The minimal sensitivity to N indicates that the self-gain of the "unit-sized" transistor is width independent. The "unit-sized" transistor can be used in a width-independent g_m/I_D design flow.

B. 4-Bit DAC

Current steering digital to analog converters (DACs) are used in communication applications. A 4-bit binary weighted DAC using the current mirrors discussed in Section IV-A is shown in Fig. 9 in order to validate the procedure developed in Section III. The steering of current generated by each current mirror is controlled by the binary bits (b_3, b_2, b_1, b_0). b_0 is the least significant bit (LSB). b_3 is the most significant bit. The currents controlled by the switching pairs are I, $2I$, $4I$, and $8I$ as indicated in Figure 9. I_L is the output current. The stress option is enabled and disabled in the simulation in order to assess the effect of stress on the input-output transfer

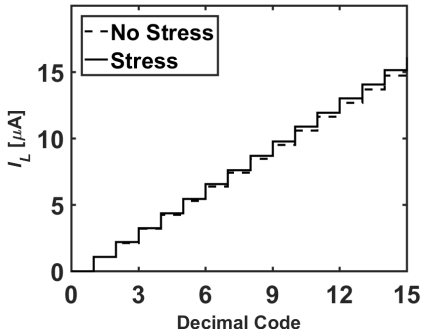


Fig. 10. Simulated input-output transfer characteristic of the 4-bit DAC. The stress option is enabled and disabled in the simulation in order to assess the effect of stress.

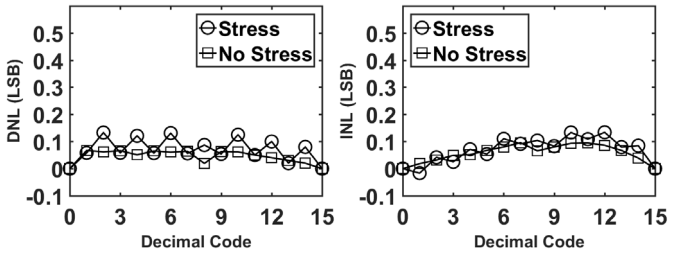


Fig. 11. (a) Differential non-linearity error and (b) integral non-linearity error of the 4-bit current steering DAC.

function, differential non-linearity (DNL) error, and integral non-linearity (INL) error.

Figure 10 shows a plot of the input-output transfer characteristic of the 4-bit DAC. The largest error due to stress occurs when all the binary bits are set to '1'. The full scale error is defined as the error of the full scale output current from the ideal full scale output current. The full scale error with the stress option enabled is 1.12 LSB. The full scale error with the stress option disabled is 0.73 LSB.

Figure 11 shows the differential non-linearity error (DNL) and the integral non-linearity error (INL) for the 4-bit DAC designed using the "unit-sized" transistor. The stress-induced error in both DNL and INL is less than 0.1 LSB when the "unit-sized" transistors are used. This result indicates that even though the procedure described in Section III does not capture layout dependent effects such as the well proximity effect and oxide-to-oxide spacing, it nonetheless provides circuit designers with a procedure to design "unit-sized" transistors capable of minimizing effects due to stress and small geometry effects.

V. Conclusion

Small geometry effects have become increasingly important in analog circuits as transistors continue to shrink. In this brief, it is shown that g_m/I_D parameters are no longer width independent when small geometry effects are considered. A procedure to develop length-specific "unit-sized" transistors that reduces the impact of the inverse narrow width effect and shallow trench isolation induced stress is proposed. It is shown that by using the "unit-sized transistors," the impact of stress on g_m/I_D dependent parameters such as current density and self gain can be reduced to 3.6 percent and 1.5 percent, respectively. Furthermore, the impact of stress on a 4-bit DAC is reduced when "unit-sized" transistors are used. The procedure described in this brief is general and can be used to redesign critical transistors affected by small geometry effects.

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